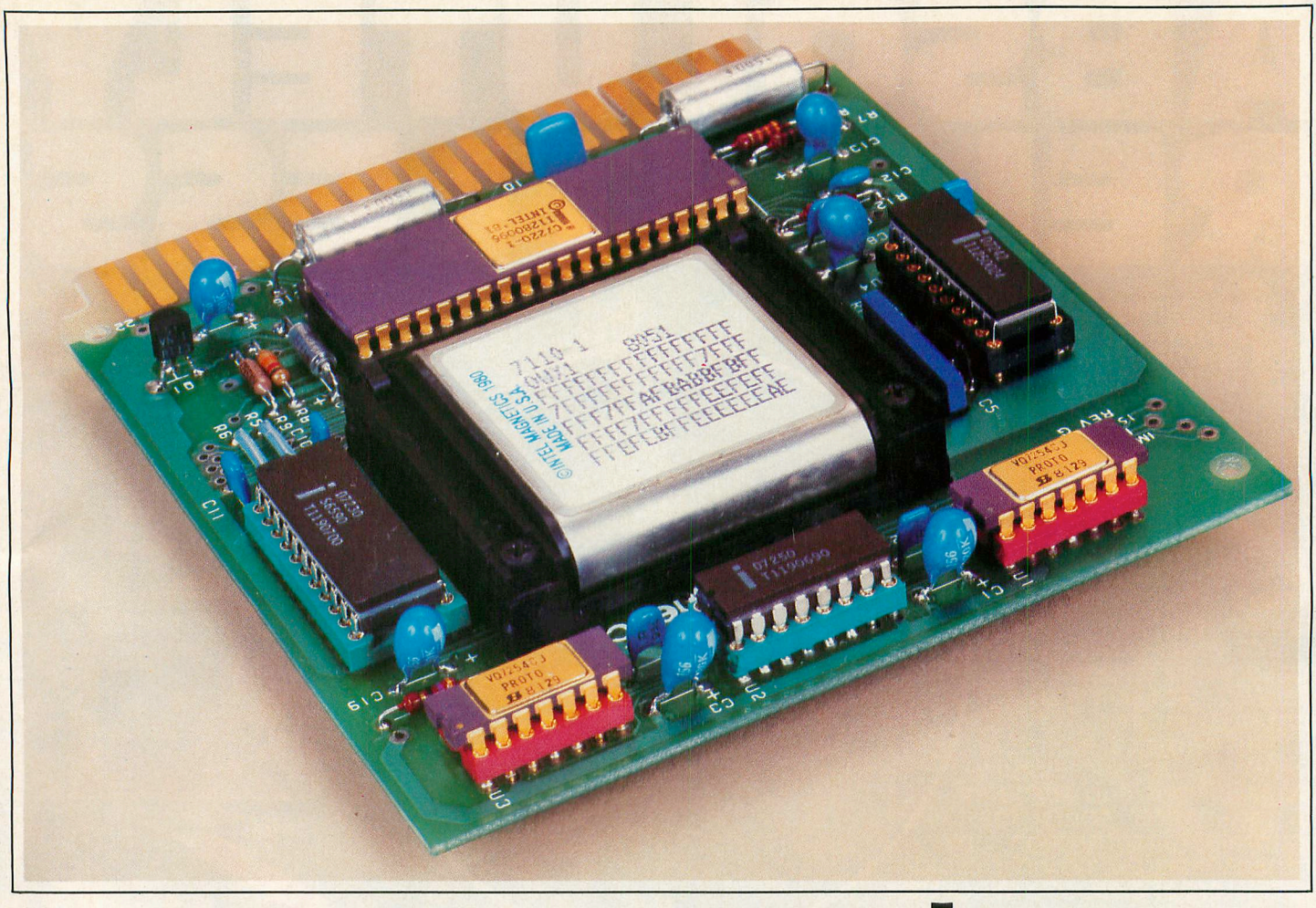


Custom Color

Try 128K bubble memory on for size.

by Dennis Kitsz

I'LL TELL YOU right from the start: This project is expensive. But, yes, *this project is* worth it. Surprisingly, it isn't complicated, but it's more sophisticated than any other peripheral for your Color Computer. What is it? The long-heralded, and finally accessible, bubble memory.

This month's article contains a lot of technical information, and if you are one of those folks who thought integrated circuits were at last beginning to make sense, get ready for an entirely new world of technology. Although bubble memory can be made to act like an ordinary computer device, it bears little electronic resemblance to familiar circuitry. It uses mysterious concepts such as "magnetic domains," and refers to coils and chevrons and synthetic garnet.

Nevertheless, you can build this month's bubble memory project and avail yourself of 128K bytes of thoroughly crash-free storage. Before you heat up those soldering irons, though, let's talk theory.

Mysteries of the Bubble

We've all played with magnets, and you can probably remember those days in science class when you slipped a piece of paper over a horseshoe magnet and dumped iron filings on the paper. Some stood up; others huddled together, forming elegant magnetic patterns on the paper. These are the familiar north-south representations of magnetic force. Yet at the minute, molecular, crystalline level, magnetism behaves curiously. A thin wafer of matter has its magnetic polarities flattened out; random, poorly differentiated areas of magnetism are found floating through the wafer. If an external magnetic field is created above and below the thin material, the magnetic areas attempt to come to attention, forming somewhat more regular (but smaller), pools. You might consider it akin to patterns of vegetable oil on the surface of a pot of water. As the oil breaks into smaller puddles, the puddles increase in regularity. If the puddles of oil are broken up vigorously, they become tiny, even circles. Likewise, when the magnetic forces above and below the thin wafer of matter (garnet crystal, in this case), are made strong enough, the magnetic areas form tiny, regular bubbles. These regular bubbles can be tamed, and, by alternating the character

Continued on page 19

Technical Background

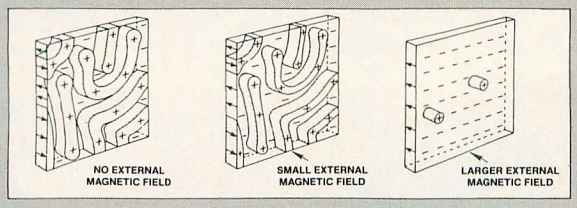


Figure A. *Magnetic bubbles are formed in a thin film of certain crystalline materials as the external magnetic field is increased.*

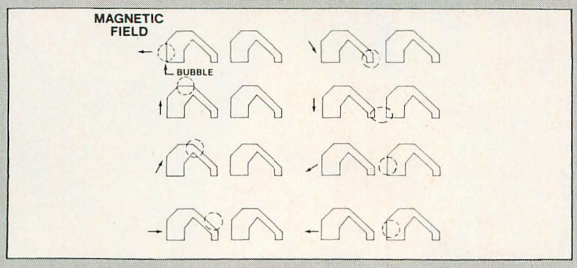


Figure B. *Bubbles are propagated around asymetrical chevrons by a rotating magnetic field; the bubbles move with the field from an area of lesser magnetism to an area of greater magnetism.*

The magnetic bubble memory is a unique solid-state storage technique, combining a century-old technology of electromagnetic wire coils (for bubble motion), analog sensing (for reading the bubbles), familiar but recent digital electronics (for interfacing), and a thin film of magnetic material (where the bubbles themselves exist).

Intel's "Primer on Magnetic Bubble Memory" (available at no charge from the Intel Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051), describes magnetic bubble memory this way:

"A magnetic bubble memory stores data in the form of cylindrical magnetic domains in a thin film of magnetic material. The presence of a domain (a bubble), is interpreted as a binary 1, and the absence of a domain is a 0. Bubbles are created from electrical signals by a bubble generator within the memory, and reconverted to electrical signals by an internal detector.

"Externally the memory is TTL-compatible.

"An external rotating magnetic field propels these cylindrical domain bubbles through the film. Metallic patterns or chevrons deposited on the film steer the domains in the desired directions. Transfer rates, once started, are in the tens of thousands of bits per second, but because the data circulates past a pickup point at which it becomes available to the outside world, there is a latency averaging tens of milliseconds before data transfer can begin.

"In these respects, magnetic bubble memories are serial high-density storage devices like electromechanical disk memories. However, in a disk, the stored bits are stationary on a moving medium, whereas in the magnetic bubble memory the medium is stationary and the bits move."

This is an excellent summary, although it's hard to imagine exactly what the bubbles are and how they move.

Magnetic materials — that is, materials which can be magnetized — contain random patterns of magnetic areas called domains. Domains are present in wrenches and cassettes, screws and loudspeakers. By magnetizing this material, the domains can be forced into patterns pointing in one direction. These large domains don't themselves move, but in a sense reorganize in a common direction. The material is then considered magnetized.

In very thin films of some kinds of crystalline matter (less than one-thousandth of an inch thick), the magnetic domains are all perpendicular to the wider expanse of the film (Figure A). That is, their poles are oriented toward either the top or bottom surfaces of the crystal wafer. At this point (before being magnetized), since because of the thinness of the wafer they seem to have no third dimension, their linear shape can be described as snakelike. By creating a permanent magnet sandwich above and below the wafer, four stages of magnetization can be made to occur. Under a weak magnetic field, all the perpendicular magnetic domains will orient their polarity in one direction — all the snakes will "belly up." As the external field is increased, the domains will shrink in width and length. An even stronger field will cause the domains to contract into cylinder shapes (which look like bubbles from above). At the extreme, the bubbles will disappear completely as the entire crystal wafer becomes evenly magnetized at its surface.

It is the third, cylindrical state which is important. This bubble domain can be made to move from an area of less magnetism to an area of greater magnetism. Intel's technique for bubble motion involves depositing asymetrical, V-shaped magnetic patterns (chevrons) on the surface of the thin film (Figure B). By means of rotating the magnetic field (by changing the current pulses in a pair of perpendicular electromagnetic coils surrounding the wafer), the bubble is forced to follow the magnetism induced in the chevron. The bubble is led around the chevron from its thick side to its thin side. As the magnetic field continues to rotate, the bubble finds itself at the end of the "V" leg with nowhere to go. It begins to stretch out, and the bubble is plucked from the thin chevron leg by the stronger field of the neighboring thick chevron leg. It continues around the new chevron, as the pattern repeats itself. The bubbles move.

Reading the moving bubbles is similar to reading the data from a disk. The bubbles are first replicated (split into duplicates) and placed on an output loop. A magnetoresistive detector — similar to a tape recording head — senses the moving bubbles and sends the information through amplification and shaping circuitry. The sense amplifiers and other external ICs organize the information into data usable by a microprocessor.

Writing data to a bubble involves taking new bubbles created at the input loop, and swapping tracks with an existing loop. The previous loop is then bumped out the end of the input track, where it is lost. The new data continues in the storage loop.

Bubble memory is unique because it is said to be non-volatile; at first it is difficult to understand why. The answer lies in the fact that permanent magnets are an integral part of the bubble memory package, keeping the magnetic domains upright and in place. If power fails, the only change to the existing situation is that the fluctuating electromagnetic field pulses which move the bubbles around simply stop. If data is being read at the time, it is merely a duplicate residing in the output track, not the original. If data is being written, only the swap time — a few microseconds — is critical. Power-fail detection circuitry keeps the swap going until it is complete.

Bubble memory is so stable, in fact, that you can remove the bubble from its socket when you are finished with it and take it with you.

Continued from page 16

of the magnetism nearby, they can be jostled around the crystal in a predictable manner. In fact, with just the right amount of bumping, the bubbles can be made to resemble nothing less than binary information!

Not convinced? Well, I guess I'm skeptical too, but bubble memories are just too expensive to chop up to see what's inside. My sales brochure from Intel Corporation has lots of pretty pictures of bubble memories being created by white-clothed lab techs, so for now I'll just accept that as true.

The technological trick to bubble memory is getting the magnetic domains to behave. There are over one million of them to keep track of, and unlike disks or other conventional (read that as "reasonable"), devices, it's the *bubbles* that move while the rest of the device stays still!

I'm hard put to come up with an analogy for exactly what goes on inside the bubble devices. You can imagine the process as a kind of micro-magnetic slam dancing. You crash into someone just as they turn to the beat, flinging you into someone else. You're the bubble, the someone else is a chevron-shaped pattern of magnetizable material deposited on the surface of the garnet, and the beat is a constantly alternating magnetic field surrounding the whole business. A field of just the right strength can slide a magnetic bubble from one chevron to the next.

What then? Why, the passing bubbles are duplicated into short "loops" to be read by an output track, amplified and shaped into proper digital signals. It's very similar to reading information on a disk, or playing back any kind of magnetic recording. A sense and read amplifier provides this good digital signal to the bubble controller chip — a sophisticated integrated circuit in the same class as disk controllers. The bubble controller assembles the information into bytes, which are provided upon request to the computer.

The data writing process is similar. Information is assembled by the bubble controller, provided to the coil driver amplifiers and power transistors, and embedded in the bubble's reserved input loop or track. At the proper time, the input loop is duplicated (by swapping the magnetic domains), into the selected loop in the main storage area.

All this provides a memory device which is environmentally stable, unaffected by power loss (since the permanent magnets in the bubble are responsible for maintaining the memory), compact (the 128K bubble is 1 1/2 inches square), and significantly faster than disk or tape storage.

The Color Interface

The circuit described this month allows the TRS-80 Color Computer to be interfaced to an Intel BPK-72 bubble memory prototype kit. Details on purchasing this kit (about $300), or a complete Color Bubble system, are provided at the end of the article.

Interfacing the BPK-72 to the TRS-80 Color Computer turns out to be a fairly simple hardware task. The bubble controller — the main communication device between computer and bubble — requires just two addresses from the computer's memory map, plus the usual reset, read/write and data signals, all available at the Color Computer's cartridge connector. A power supply (5 and 12 volts) is also needed, together with a 4 MHz clock used for bumping along the magnetic domains within the bubble memory system. The rest of the system's operation is handled in the software.

Before beginning this project, please take note of several things:

- The Color Bubble system costs more than the entire computer, and each 128K bubble is an additional $100 investment. That means it is not an economical replacement for disk storage, but can act most effectively as a kind of extended RAM or fast-access storage compartment for a dozen of your best programs.
- The Color Bubble needs an operating system before it can function. A bubble operating system can be extremely rudimentary or as sophisticated as the best disk operating systems on the market. Jake Commander is working on one that you'll find in **The Color Computer Magazine** in the next month or so, and is putting finishing touches on The BOSS (Bubble Operating System Software), a high-powered interactive system.
- The Color Bubble is only one part of a coherent system of Color Computer peripherals which are being presented regularly in this column. Hence, the address decoding is taken from the group of phantomed addresses found in the disk area. Refer to Custom Color, April and May 1983 columns for details. In this case the addresses are selected by demultiplexer circuit U5, and provided, through suitable decoding, to the type 7220 bubble controller chip on board the Intel BPK-72 bubble memory kit.

An operating system — or at least a bubble "boot" — must be provided so the unique machine language commands of the bubble controller chip can be embedded in the Color Computer's Basic language. It can be typed in, loaded from tape, or (best of all), be present in a ROM of some kind. The bulk of the operating system can be contained in the bubble itself, but something must boot that operating system in place when the computer is turned on. Figure 1 is the complete schematic for the bubble interface and for an operating system EPROM (a standard 2716 or 2732 erasable memory).

For those interested in a single-board, hard-wired system — including the I/O port from April and May, and the upcoming EPROM programmer, real-time clock, and other circuits — the select signals (marked W, X, Y, and Z) are ORed for feeding through. Optionally, the 74LS139 may be left out of subsequent boards, and the select signals taken from the first board plugged in place (normally the I/O board), or from a motherboard of some kind. Plans for a completely buffered motherboard will be provided in a later column. In the meantime, you can socket the 74LS139 for later removal if you build the motherboard system.

The Intel Bubble System

The history of bubble memory is filled with starts and stops, of announcements and failures, and of companies investing huge sums of money only to sooner or later drop out of the technological race. Despite several years of research, then, bubble memory is still in its infancy. This in turn leaves a standardization gap to be filled; that, alas, is in the future.

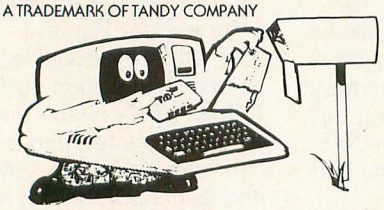
With several competing systems now available — none compatible with any other — I found it necessary to choose only one to work with; I selected National Semiconductor. After two months of work, I opened Electronic Engineering Times to discover that National had dropped its bubble memory division; the telephone number I had used the day before was disconnected. Remaining were Fujitsu and Intel, and a wave of patriotism came over me. I selected the Intel product, which turned out to be stable and reliable, though more expensive than Fujitsu's bubble.

The Intel bubble memory product comes in several forms, including individual components and complete boards and systems. The interface presented in this article connects the Color Computer to the Intel BPK-72 prototype kit. This kit, available from Intel distributors, consists of: a type 7110 one-megabit magnetic bubble memory; a 7250 coil predriver; two 7254 quad VMOS drive transistor arrays (for alternating the pulses in the bubble memory coils); a 7230 current pulse generator; a 7242 formatter/sense amplifier (for reading the boot loop); a

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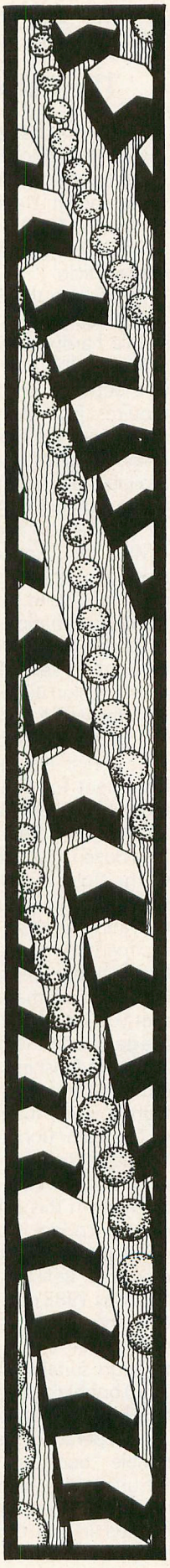
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Continued from page 19

7220 magnetic bubble memory controller (to interface with the computer); power-fail detection circuitry; a circuit board; and all parts and documentation. Also included are a dummy module, necessary for testing the proper operation of the circuit board before inserting the costly bubble memory itself; and a seed module, needed for re-seeding the bubble if the boot loop information is accidentally erased.

The BPK-72 is fairly straightforward to build, although it is no Heathkit project. Intended as an evaluation board for engineers, the BPK-72 contains a schematic diagram and parts layout, but no step-by-step instructions or construction hints. The process is complicated slightly by a series of changes made to the BPK-72 printed circuit board which were not reflected in the documentation provided with it. Although Intel has promised to update the documentation, as of this writing it remains unchanged. When constructing the BPK-72, then, be aware of the following changes to the Revision H circuit board (Figure 2):

1. C18 has been changed from a ceramic to an electrolytic capacitor of the same value. Be careful to note the correct orientation of this capacitor.
2. R8 has been changed from 12K to 1K.
3. The melt-on socket has been replaced by a screw-down socket.
4. The unidentified parts on the circuit board are:

U8	75463 integrated circuit
R17	3.9K, 1/4 w
R18	5.6K, 1/4 w
R19	5.1K, 1/4 w
C20	.01 mF, ceramic
C21	.01 mF, ceramic
CR1	1N914 diode
CR2	1N914 diode

To construct the BPK-72, install the sockets, then the small parts, and finally insert all the integrated circuits, except the 7110 bubble. When construction is complete, set the BPK-72 aside and begin work on the interface.

Bubble Interface Construction

You can choose any method for wiring the interface (point-to-point or wire-wrap), which is not a complicated task (Figure 1). I recommend using the Radio Shack prototyping boards (276-163 $4.95 or 276-165 $9.95), which are more than convenient, since they are made to plug directly into the comput-

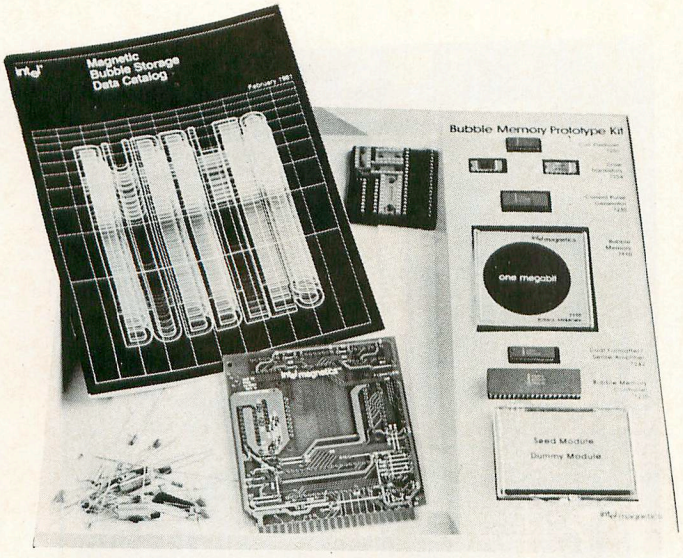


Photo 1. *The Intel BPK-72 bubble memory prototype kit contains the complete data, all integrated circuits and test modules, small parts and sockets, and a high-quality printed circuit board.*

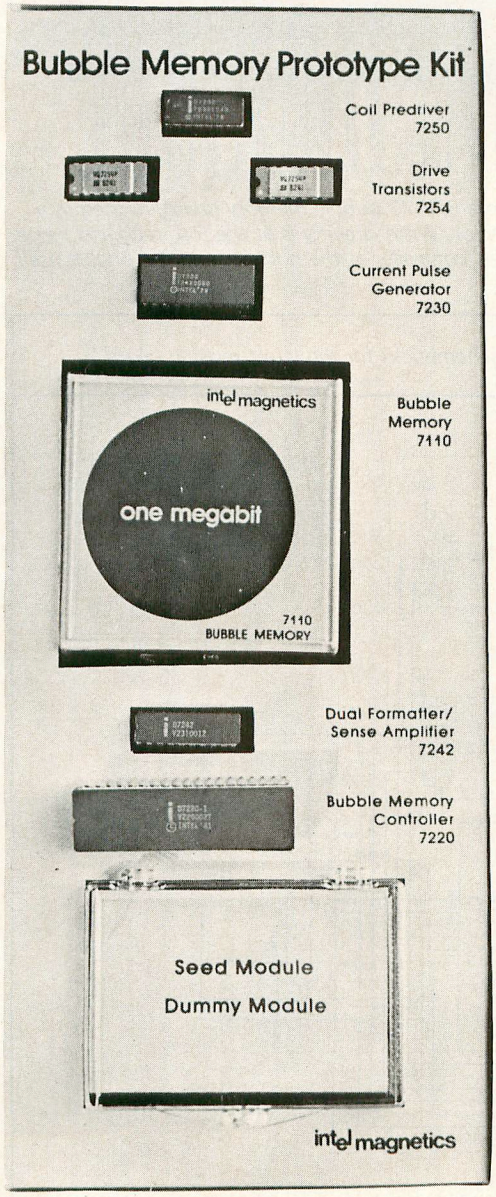
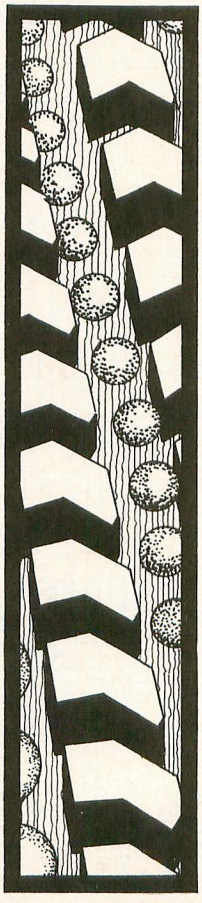


Photo 2. *Complete integrated circuit set provided with the BPK-72 includes the bubble memory, five peripheral chips, bubble memory controllers, and test modules.*



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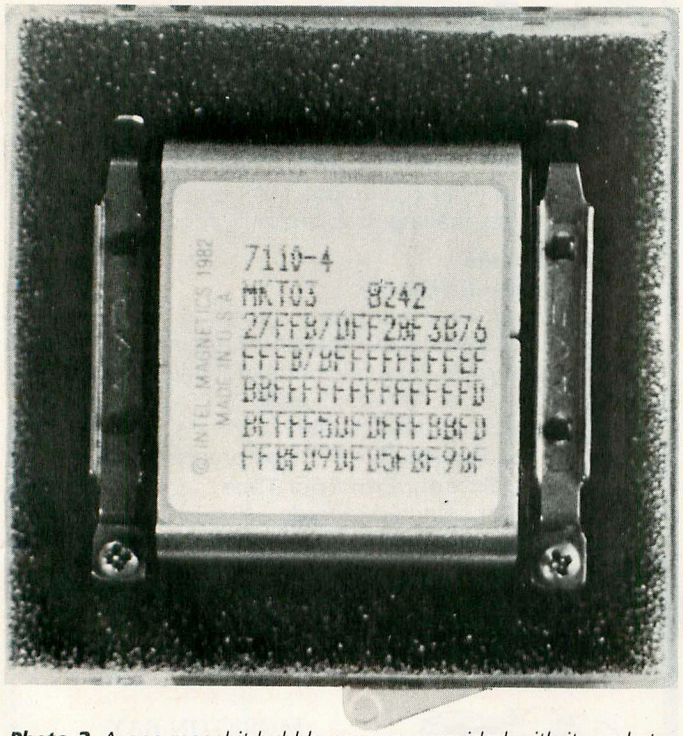


Photo 3. *A one-megabit bubble memory, provided with its socket. The information printed on top is a map of the good loops inside the bubble. At this early stage of bubble technology, 25 percent additional bubble loops are provided for redundancy, guaranteeing 100 percent quality of the final memory. Should seed information be erased by the user, the map allows it to be restored using the seed module, for use by the format/sense amplifer.*

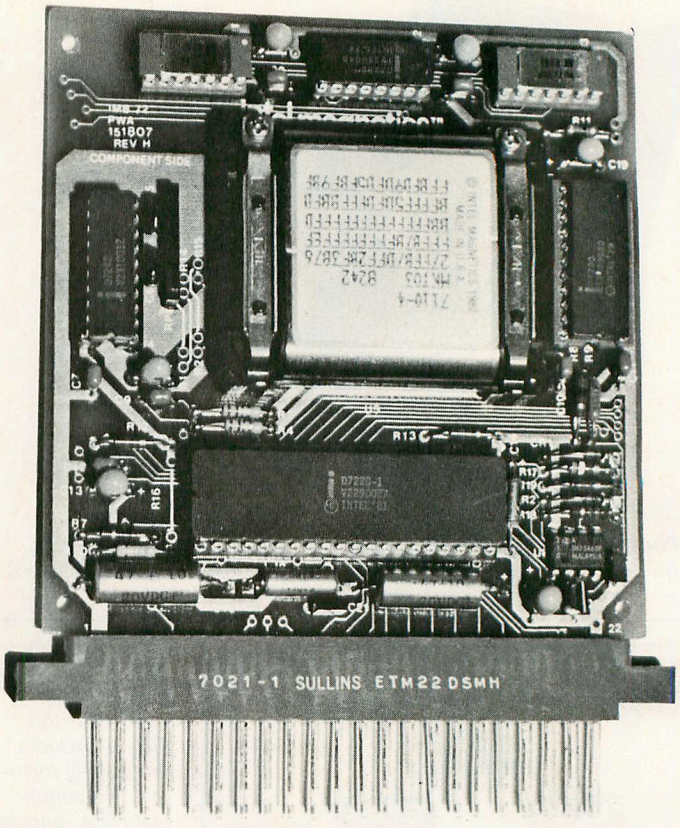
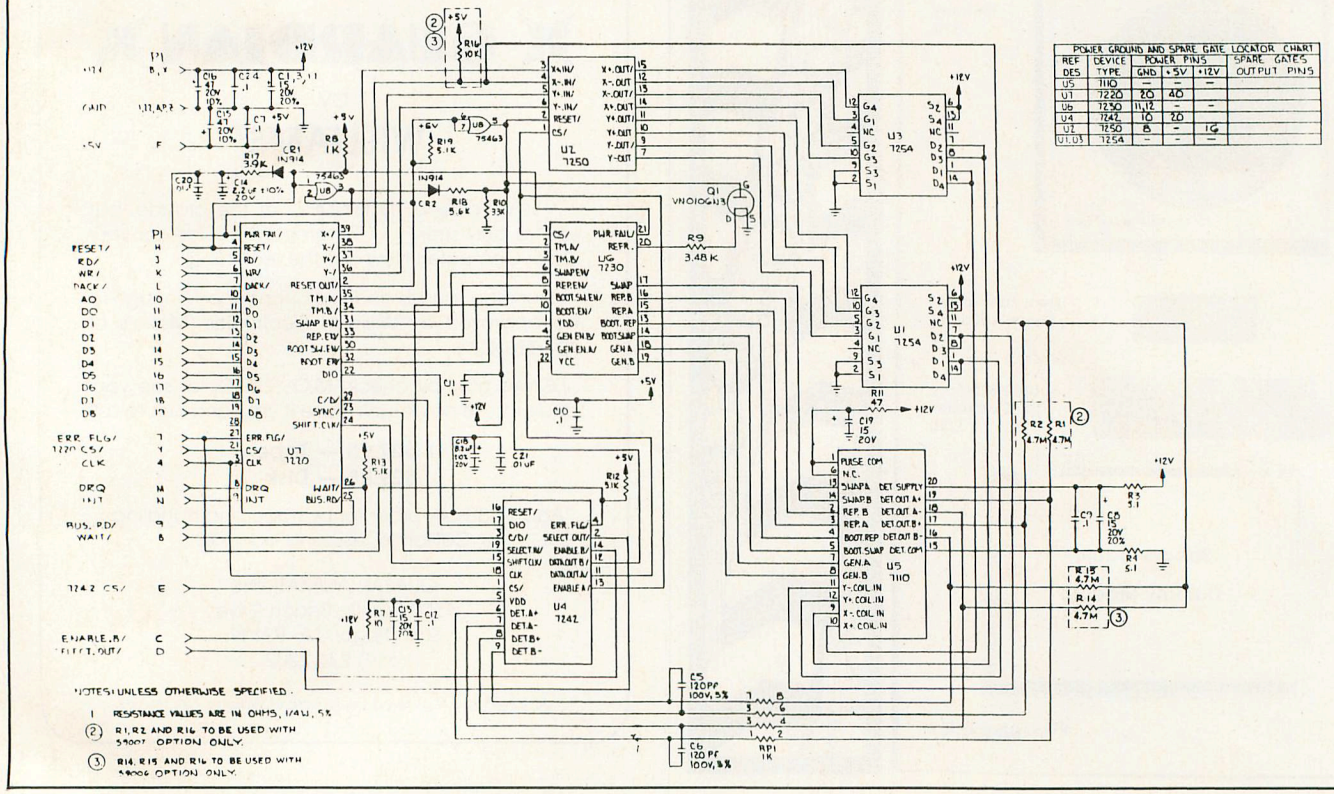


Photo 4. *A complete BPK-72 bubble memory board inserted in a 44-pin edge connector. Write circuitry is at the top, read and sense circuitry at the sides, controller at the bottom, and the bubble itself in the center.*

Figure 2. *Schematic for the BPK-72 bubble memory board made by Intel. This schematic is for the latest revision board.*



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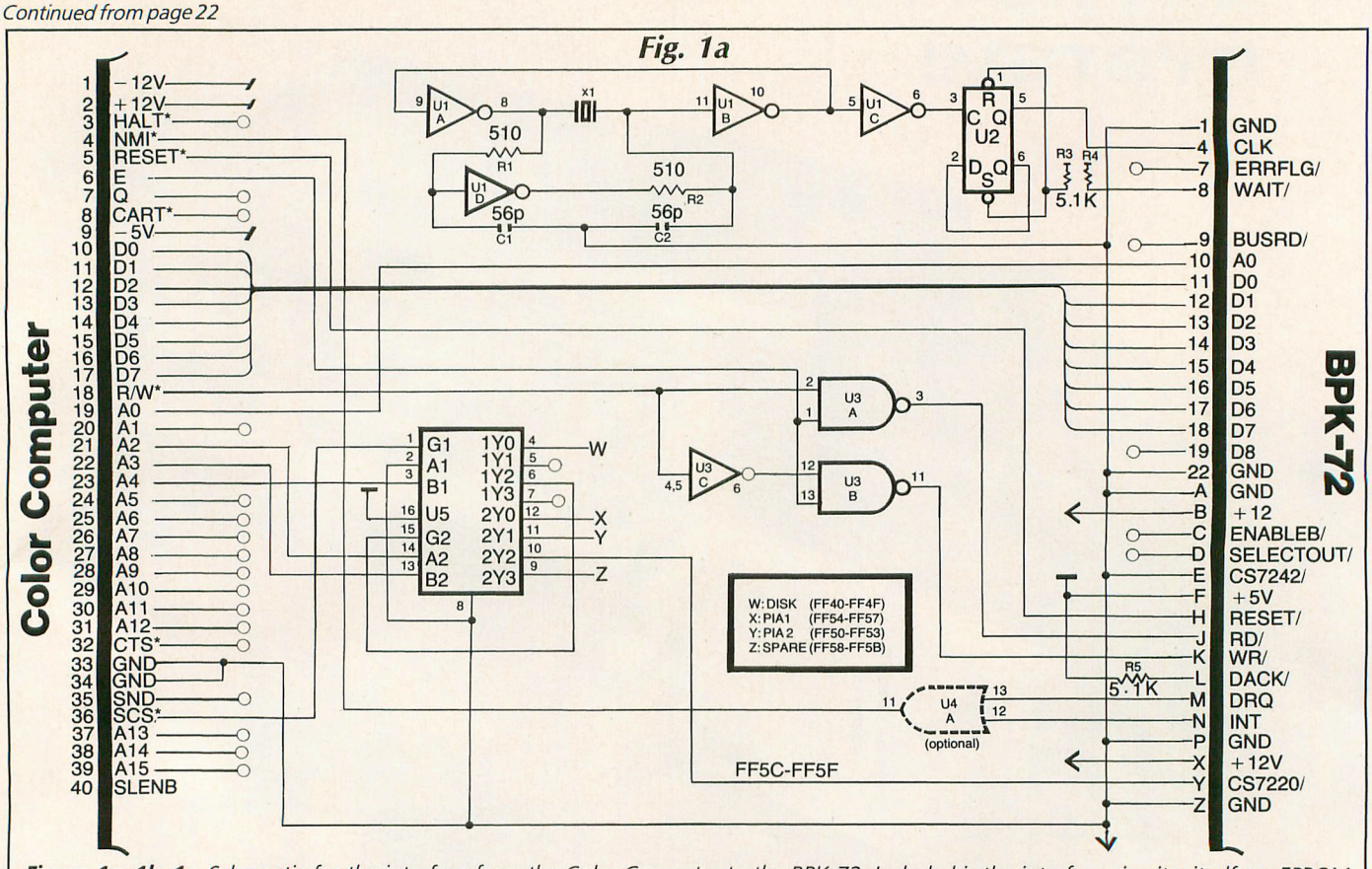


Figure 1a, 1b, 1c. *Schematic for the interface from the Color Computer to the BPK-72. Included is the interface circuitry itself, an EPROM for containing the bootstrap and system programs, and an optional interrupt signal.*

Summer Programming Project

We decided to give you something to do this summer: write an original game for the Color Computer. It can be an adventure, simulation, arcade, or any type of game imaginable. It can be written in Basic or assembly language. It can be long or short, it's all up to you. Just make sure you get it to us by Labor Day, September 5, 1983.

Entries should be submitted on cassette tape or disk with clearly written instructions for use. All entries will be held until October 1, 1983. For the return of entries not selected for prizes, include a self-addressed stamped envelope with you program. All winners will be announced in December's issue of **The Color Computer Magazine**. Entries will be judged by **The Color Computer Magazine**'s editorial staff. All decisions are final.

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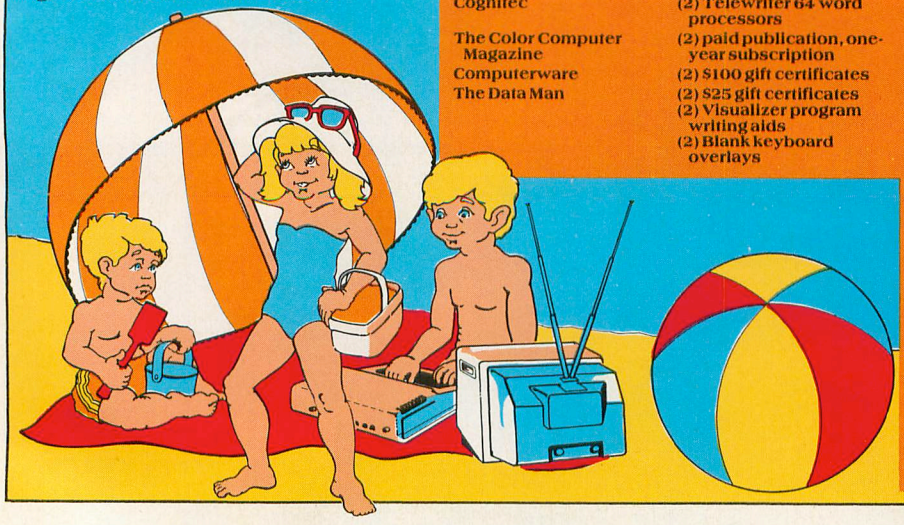


Fig. 1b

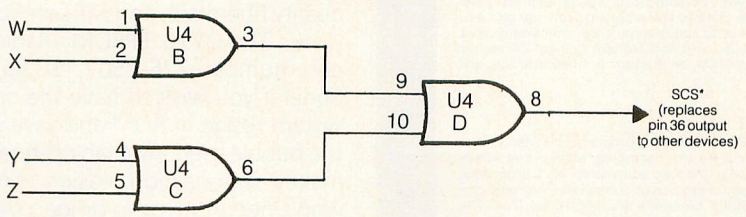
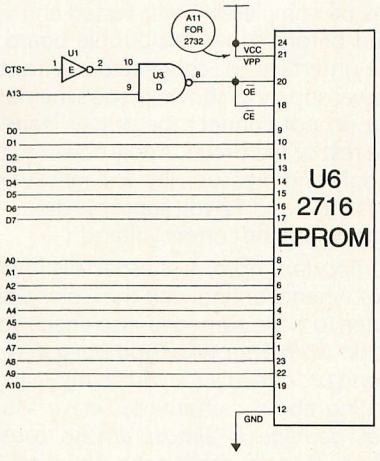


Fig. 1c



A0	D7	D6	D5	D4	D3	D2	D1	D0	Symbol	Name of Register	Read/Write
1	0	0	0	1	C	C	C	C	CMDR	Command Register	Write Only
1	0	0	0	0	B	B	B	B	RAC	Register Address Counter	Write Only
1	S	S	S	S	S	S	S	S	STR	Status Register	Read Only

SSSSSSSS = 8-bit status information returned to the user from the STR
CCCC = 4-bit command code sent to the CMDR by the user.
BBBB = 4-bit register address sent to the RAC by the user.

Table 1. *Register addressing of the 7220 bubble memory controller (overview).*

RAC A0	B3	B2	B1	B0	Symbol	Name of Register	Read/Write
0	1	0	1	0	UR	Utility Register	Read or Write
0	1	0	1	1	BLR LSB	Block Length Register LSB	Write Only
0	1	1	0	0	BLR MSB	Block Length Register MSB	Write Only
0	1	1	0	1	ER	Enable Register	Write Only
0	1	1	1	0	AR LSB	Address Register LSB	Read or Write
0	1	1	1	1	AR MSB	Address Register MSB	Read or Write
0	0	0	0	0	FIFO	FIFO Data Buffer	Read or Write

B3B2B1B0 = 4-bit contents of RAC at the time the user makes a read or write request with A0 = 0.
LSB = Least Significant Byte
MSB = Most Significant Byte

Table 2. *Register addressing of the 7220 bubble memory controller (detail).*

D3	D2	D1	Do	Command Name
0	0	0	0	Write Bootloop Register Masked
0	0	0	1	Initialize
0	0	1	0	Read Bubble Data
0	0	1	1	Write Bubble Data
0	1	0	0	Read Seek
0	1	0	1	Read Bootloop Register
0	1	1	0	Write Bootloop Register
0	1	1	1	Write Bootloop
1	0	0	0	Read FSA Status
1	0	0	1	Abort
1	0	1	0	Write Seek
1	0	1	1	Read Bootloop
1	1	0	0	Read Corrected Data
1	1	0	1	Reset FIFO
1	1	1	0	MBM Purge
1	1	1	1	Software Reset

Table 3. *The 16 commands of the 7220 bubble memory controller. For details of the use of the commands, refer to the 7220 data sheet or application notes (packed with the BPK-72 kit).* *Please turn to page 26*

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Continued from page 25

er's 40-pin, 0.1-inch spaced, female edge connector. These boards are high-quality fiberglass, and will save you much work. The 2716 EPROM (Radio Shack part number 276-2507, $6.95) is optional if you wish to have the operating system reside in ROM and save space in the bubble itself. Also, an on-board ROM makes initialization easier, since you won't need to type in or load from tape the bubble operating system bootstrap routine.

The most critical part of this construction project is the power supply. Although quite simple, it is important that this be completely built, tested and verified before either the bubble board or the interface is connected. Wire the power supply as shown in the schematic, but do not connect the power leads to the rest of the circuit. Apply power to the supply and measure the voltages. Verify that the 5 and 12 volt supply sections are putting out the correct voltage.

Important note; It is especially important when working with the Color Computer to have someone else check your work. *No matter what you build, have a friend proofread it for you.* In my years of writing about computers, I have found that *damage is almost always caused when readers don't take the time to proofread their work.* Do it. Save yourself the aggravation and me the time it takes to answer your letter.

When the power supply is working, wire the remainder of the interface. If you choose to include the EPROM, wire this section first. If you have an EPROM already programmed with any information at all, put it in the EPROM socket, and insert the interface in the Color Computer cartridge slot. Power up the interface first, then the computer, and PEEK through memory locations starting at $E000 (57344 decimal) to assure yourself the information is there. Remove the interface and complete the construction.

Again test the unit by inserting the interface, powering up the computer, then the interface, and verifying that all computer operations are normal. *If at any time the computer locks up or fails to operate properly, immediately turn it and all peripherals Off!* The central processing unit of the Color Computer is unbuffered and delicate; remember to have someone else check your work.

Testing Your Bubble System

By this time you should have a complete, working interface, and an assem-

Listing 1. *Bubble memory test routine, to be used before insertion of the 7110 bubble memory.*

```
10 CLS : PRINT"Bubble Memory Test Routines" : PRINT
20 PRINT"Use the dummy module, not the 7110!" : PRINT
30 D=&HFF5C : S=&HFF5D : REM * D=DATA S=STATUS
40 POKES,11 : POKED,1 : POKED,16 : POKED,8 : POKED,0 :
   POKED,0 : P=PEEK(S) : PRINTP" = current status" : IF
   P=64 THEN PRINT"This value is correct" ELSE PRINT "This
   value should be 64" : REM * Set up 7220 controller
60 GOSUB 1000
70 ON A GOTO 80,40
80 CLS : PRINT"Beginning next test..."
90 FOR X = 1 TO 40 : POKED,X : NEXT : REM * Fill 7220
   byte buffer
100 P=PEEK(S) : REM * Again check status
110 IF P=41 THEN PRINT"Bubble buffer full; continuing"
    : GOTO120 : ELSE PRINT"Bubble buffer status bad." :
    PRINT"Trying again" : GOTO 90
120 PRINT"Now reading buffer..."
130 FOR X = 1 TO 40 : PRINT PEEK(D); : NEXT : REM * Read
    back bytes from 7220
140 PRINT : PRINT"The above should read 1 to 40"
150 GOSUB 1000
160 IF A=1 THEN 170 ELSE 120
170 PRINT"Initial interface tests complete."
180 GOSUB 1000
190 IF A=1 THEN RUN ELSE END
1000 PRINT"(C)ontinue or (R)epeat Test"
1010 A$=INKEY$ : IF A$="C" OR A$="c" THEN A=1 : RETURN
1020 IF A$="R" OR A$="r" THEN A=2 : RETURN
1030 GOTO 1010
```

bled BPK-72 bubble memory board with all integrated circuits installed except the 7110 bubble memory itself. Put the dummy module in the socket; note that the socket provided is a newer Augat type that opens by loosening two screws. Lift up the socket locking arms, drop in the dummy module (there is a small notch to guide it to the correct orientation), and relock and screw down the arms.

Connect the boards together and apply power (the boards are not yet hooked to the computer). Verify that the voltages are still correct, and that they are present on the BPK-72 board as noted in the schematic. Remove the power, wait a short time for the capacitors to discharge, insert the complete unit into the computer, power up the computer, power up the interface, and refer to Listing 1.

The listing is a short Basic program that runs the interface and bubble controller through their paces. It will verify the proper operation of the bubble system as a whole by reading from and writing through the controller chip, which cannot operate correctly without: proper addressing from the interface; correct clock frequency from the interface; accurate information from the format/sense amplifier; *and* a stable power supply.

If it passes this test, you're ready to continue. If not, stop now and recheck all your work! Here is a quick checklist of places to look:

- Are all solder joints made on both boards?
- Are all wires connected (if you used a wire-wrap or point-to-point technique)?
- Are all solder joints good (shiny)?
- Are the boards inserted straight?
- Is either board inserted backwards?
- Are all ICs inserted in the correct direction?
- Are any pins crushed under ICs?
- Are any pins slipping out the sides of sockets?
- Are ICs in the proper sockets on both boards?
- Does the power supply still test okay?
- Are all resistors installed on the interface?
- Is polarity correct on all BPK-72 electrolytic capacitors?
- Does any part get very hot?

Once you have corrected any problems, your board should pass the test program, since the interface is simple and the bubble board is extremely reliable. The final step is recommended but not absolutely necessary if your soldering and assembly technique is good; the most damage you can cause is to lose the seed information from the bubble, which is printed on the top of the bubble itself and can be restored at any time. To avoid the possibility of this inconvenience it is wise, before inserting the 7110 bubble memory, to verify that all the coil drive signals are occurring at the proper times and voltage levels. Prepare the program in Listing 2 on an Editor/Assembler (EDTASM+ or equivalent), or use the Basic program in Listing 3. Running this program will produce a continuous stream of coil pulses, which can then be displayed on an oscilloscope. Figure 3 presents the waveforms that must be visible on the 7110's socket pins.

The details on the interpretation of these signals are found in Intel's application note AP-119, on page 18. This information is provided with the BPK-72 kit, so if your waveforms don't come close to those shown in the figure, be sure to refer to this note. If everything checks out fine to this point, you're ready to use the bubble memory.

What's It Good For?

When considering this project I asked myself, why would anyone want to spend $350 or more to have bubble memory? Why not just have a disk drive for the same price?

The most important answer for me is experience: What have I done over time with my two Model I disk drives?

Actually, it turns out I only use one of them in true read/write fashion — drive 0 simply contains all the utilities, such as Electric Pencil, Scripsit, Disk Basic, Superzap, and about 15 others on a write-protected disk. I seldom change the disk; drive 1 gets the workout.

In effect, my bubble memory becomes drive 0. It's 128K can contain your utilities, plus any other frequently used information. Since it is so fast, it acts like you have the programs in RAM. From my per-

Please turn to page 30

Listing 2. *Assembly listing of control signal waveform generation program, used for testing the BPK-72 timing.*

```
                        00100 * A PROGRAM TO CREATE COIL DRIVE
                        00110 * SIGNALS FOR OSCILLOSCOPE DISPLAY
                        00120 *
1000                    00130          ORG     $1000
                        00140 *
1000 86   0B          00150 START    LDA     #$0B
1002 B7   FF5D        00160          STA     $FF5D
1005 86   00          00170          LDA     #$00
1007 B7   FF5C        00180          STA     $FF5C
100A 86   11          00190          LDA     #$11
```

Listing continued on page 28

Listing continued from page 27

```
100C B7   FF5C     00200          STA     $FF5C
100F 86   08       00210          LDA     #$08
1011 B7   FF5C     00220          STA     $FF5C
1014 86   00       00230          LDA     #$00
1016 B7   FF5C     00240          STA     $FF5C
1019 B7   FF5C     00250          STA     $FF5C
101C 86   12       00260          LDA     #$12
101E B7   FF5D     00270          STA     $FF5D
1021 B6   FF5D     00280 LOOP     LDA     $FF5D
1024 81   20       00290          CMPA    #$20
1026 27   F9       00300          BEQ     LOOP
1028 7E   1000     00310          JMP     START
                   00320 *
          0000     00330          END
00000 TOTAL ERRORS
LOOP    1021
START   1000
```

Listing 3. *Basic listing of the assembly program shown in Listing 2.*

```
10 DATA 86,0B,B7,FF,5D,86,00,B7
20 DATA FF,5C,86,11,B7,FF,5C,86
30 DATA 08,B7,FF,5C,86,00,B7,FF
40 DATA 5C,B7,FF,5C,86,12,B7,FF
50 DATA 5D,B6,FF,5D,81,20,27,F9
60 DATA 7E,10,00
70 A$="&H"
80 FORN=&H1000 TO &H102A
90 READB$
100 X=VAL(A$+B$)
110 POKEN,X
120 NEXT
130 EXEC&H1000
```

Glossary

bias field — a magnetic field applied to a thin magnetic film to reduce magnetic domains to bubbles.

boot loop — a special loop to map which loops are active and which are inactive, as found by factory testing.

bubble, magnetic — a cylindrical magnetic domain in a thin film of garnet; viewed from above it appears to be a bubble. It represents a binary 1.

chevron — one of many possible shapes for a metallic pattern deposited on a film of garnet to propel and steer bubbles.

detector — a device to distinguish bubbles from non-bubbles.

domain, magnetic — a small region of a ferromagnetic material containing similarly oriented atoms, so that the region is magnetized in one direction.

garnet — a naturally occuring silicate mineral. Synthetic garnet with similar crystal structure is made of oxides of lead and yttrium or other rare earths.

input track — a row of chevrons that leads bubbles from a generator to storage loop tracks.

latency — the delay between a request to read/write a memory address and the occurance of the operation, until that address arrives physically (not necessarily mechanically).

major loop — a loop with a generator, detector, or an annihilator, used to read/write data from/to a number of minor loops.

minor loop — an endless loop track for storing bubbles.

non-volatile — memory that retains data integrity with power shut off.

output track — a row of chevrons that lead bubbles from a storage loop to a bubble detector.

random access — memory whose access time to any bit is wholly independent of that bit's address.

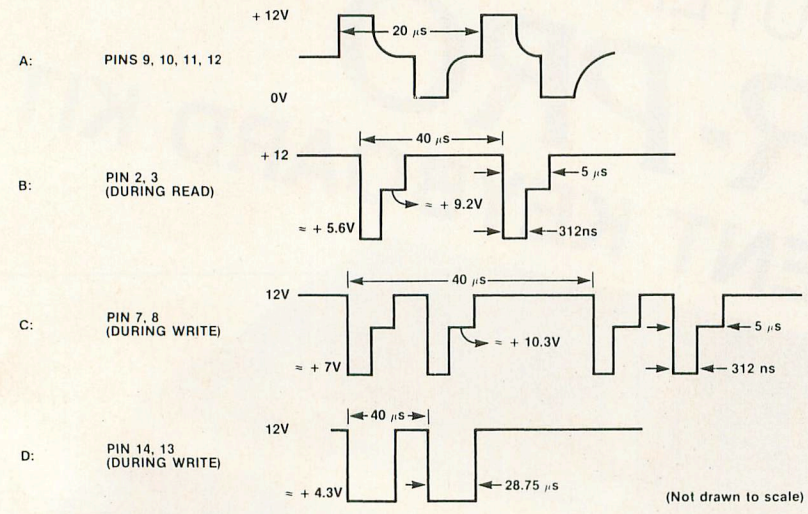
serial access — memory whose access time to any bit is very dependent on that bit's address.

Listing 4. *All the 7220 control commands written as a series of subroutines. Once your bubble memory is complete, you can use these routines to experiment with bubble operation.*

```
                        00100 *
                        00110 * 7220 COMMAND SUBROUTINES
                        00120 * EACH ROUTINE WRITES A
                        00130 * SINGLE COMMAND TO THE
                        00140 * 7220 BUBBLE MEMORY
                        00150 * CONTROLLER
                        00160 *
1000                    00170          ORG     $1000
                        00180 *
                        00190 * WRITE BOOTLOOP REGISTER
                        00200 * MASKED
1000 86   10            00210 CMND0    LDA     #$10
1002 20   3A            00220          BRA     OUT
                        00230 * INITIALIZE COMMAND
1004 86   11            00240 CMND1    LDA     #$11
1006 20   36            00250          BRA     OUT
                        00260 * READ COMMAND
1008 86   12            00270 CMND2    LDA     #$12
100A 20   32            00280          BRA     OUT
                        00290 * WRITE COMMAND
100C 86   13            00300 CMND3    LDA     #$13
100E 20   2E            00310          BRA     OUT
                        00320 * READ SEEK COMMAND
1010 86   14            00330 CMND4    LDA     #$14
1012 20   2A            00340          BRA     OUT
                        00350 * READ BOOTLOOP REGISTER
                        00360 * COMMAND
1014 86   15            00370 CMND5    LDA     #$15
1016 20   26            00380          BRA     OUT
                        00390 * WRITE BOOTLOOP REGISTER
                        00400 * COMMAND
1018 86   16            00410 CMND6    LDA     #$16
101A 20   22            00420          BRA     OUT
                        00430 * WRITE BOOTLOOP COMMAND
101C 86   17            00440 CMND7    LDA     #$17
101E 20   1E            00450          BRA     OUT
                        00460 * READ FSA STATUS COMMAND
1020 86   18            00470 CMND8    LDA     #$18
1022 20   1A            00480          BRA     OUT
                        00490 * ABORT COMMAND
1024 86   19            00500 CMND9    LDA     #$19
1026 20   16            00510          BRA     OUT
                        00520 * WRITE SEEK COMMAND
1028 86   1A            00530 CMNDA    LDA     #$1A
102A 20   12            00540          BRA     OUT
                        00550 * READ BOOTLOOP COMMAND
102C 86   1B            00560 CMNDB    LDA     #$1B
102E 20   0E            00570          BRA     OUT
                        00580 * READ CORRECTED DATA
                        00590 * COMMAND
1030 86   1C            00600 CMNDC    LDA     #$1C
1032 20   0A            00610          BRA     OUT
                        00620 * FIFO RESET COMMAND
1034 86   1D            00630 CMNDD    LDA     #$1D
1036 20   06            00640          BRA     OUT
                        00650 * MBM PURGE COMMAND
1038 86   1E            00660 CMNDE    LDA     #$1E
103A 20   02            00670          BRA     OUT
                        00680 * SOFTWARE RESET COMMAND
103C 86   1F            00690 CMNDF    LDA     #$1F
103E B7   FF5D          00700 OUT      STA     $FF5D
1041 39                 00710          RTS
                        00720 *
          0000          00730          END
00000 TOTAL ERRORS
CMND0   1000            CMND8   1020
CMND1   1004            CMND9   1024
CMND2   1008            CMNDA   1028
CMND3   100C            CMNDB   102C
CMND4   1010            CMNDC   1030
CMND5   1014            CMNDD   1034
CMND6   1018            CMNDE   1038
CMND7   101C            CMNDF   103C
                        OUT     103E
```

Continued from page 28

Figure 3. *Control signals that should be present on the 7110 bubble socket when Listing 2 or 3 is run. Use a 10-MHz oscilloscope for accurate display.*



spective, if I'm going to spend a few hundred dollars just to hold utility programs, it might as well be for the bubble system instead of a disk drive, which is slow and mechanical.

The disadvantage of the bubble is, of course, the cost of the 7110 bubble memories themselves. It's not likely you can afford to keep a shelf of them at $100 each. But then, the security of knowing your sensitive information is crash-free and protected from prying eyes might be convincing. And the cost might come down in the next few years. Intel predicts that by next year 1 megabyte of bubble storage will cost the same as 128K does today.

Updates

- Due to stresses on its supply system, Radio Shack can no longer offer the Extended Color Basic ROM at the Repair Center cost, as described in the March column. The ECB ROM will still be available on an exchange basis (only) with damaged ECB ROMs at the $67 price, and the ECB ROM kit can be purchased from Computer Centers, without installation or warranty, for $99.
- Due to quality control difficulties with external suppliers and manufacturers, projects appearing in this column will in the future be available from me directly, or from authorized dealers, under the Green Mountain Micro logo. Write to me at Green Mountain Micro, Roxbury, Vermont 05669, and ask for a catalog and dealer list.
- With reference to the above, the I/O port described in April and May should be in stock by the time you read this. My apologies for the delay. The Color Computer lowercase generator (Lowerkit), the TV Buff monitor output board, an updated Video Display Scroller, and the Bubble Memory Interface (Color Computer or Model III) are in stock.
- For the hundreds of readers who wrote asking for 64K upgrades and information on the 32K upgrades and other modifications for the newer NC-revision Color Computer, and for early C-revision boards, please have patience. I am preparing a complete rundown on this information for publication soon.
- Due to power failures during freak heavy spring snows in Vermont, this month's entire column was prepared on Radio Shack's new Model 100 portable computer. Congratulations to the Shack on their high tech breakthrough!
- During the next few months, look for plans for a complete lowercase and special character generator that fits compactly inside the Color Computer; a replacement keyboard project; an EPROM programmer; and a real-time clock. See you next month.

Bubble Memory Parts List

The BPK-72 bubble memory evaluation kit is available from Intel Magnetics, 3065 Bowers Avenue, Santa Clara, CA 95051. Contact the office of Steve Coney, NVMD Marketing, Mail Stop SC2-961; specify the BPK-72-4, which is the commercial temperature range (0 to 70 degrees C). The price is $299 for the complete kit.

The interface is available as a complete kit of parts and circuit board ($50) or assembled and tested ($100) from Green Mountain Micro, Roxbury, VT 05669, (802) 485-6112. The complete system (BPK-72, interface, and The Color BOSS — bubble operating system software by Jake Commander) is available for $550 from Green Mountain Micro.

Individual parts:

U1	74H04/F04 (*not* LS04!) hex inverter
U2	74LS74 dual flip-flop
U3	74LS00 quad 2-input NAND gate
U4	74LS32 quad 2-input OR gate
U5	74LS139 dual 2-of-4 demultiplexer
U6	2716 5-volt 2Kx8 EPROM
U7	7805 5-volt regulator
U8	7812 12-volt regulator
C1,C2	56 pF, 50V
C3	2200 mF, 50V
C4	100 mF, 35V
C5	100 mF, 35V
C6-C16	0.1 mF ceramic bypass
CR1	2A, 50V bridge rectifier
R1,R2	510 ohms, 1/4w
R3-R5	5.1k, 1/4w
T1	18 to 24 volt, 2A transformer
X1	8.000 MHz crystal

Miscellaneous: circuit board with male, 0.1-inch, 40-pin edge connector; 0.1-inch, 40-pin female card connector (for feed-through to disk, if desired); 0.156-inch, 44-pin female card connector; heat sinks for the regulators; sockets; solder; wire; hardware.

Technical Specifications

- Bubble memory manufacturer: Intel Corporation, Santa Clara, California.
- Interface manufacturer: Green Mountain Micro, Roxbury, Vermont.
- Operating system bootstrap and system routines in ROM from $E000 to $EFFF; expanded operating routines in the bubble.
- Bubble size: 1 Megabit (128K bytes), expandable by using 4 Megabit (512K bytes) bubble, which is pin-for-pin compatible. Also expandable by adding bubble (BPK-70) boards. Internal organization is 2048 loops, 512 bits/loop.
- Data transfer rate: Depending on software, up to 50K bytes per second.
- Average access time: 50 mS. System clock frequency is 4 MHz +/−0.1 percent.
- Power requirements: +12 volts, 400 mA; +5 volts, 400 mA (maximum); built-in powerfail detection.
- Operating temperature range: 0 to 70 degrees C.
- Cost: See parts list. ■■■